Inductive Adders

Pulsed Power Engineering
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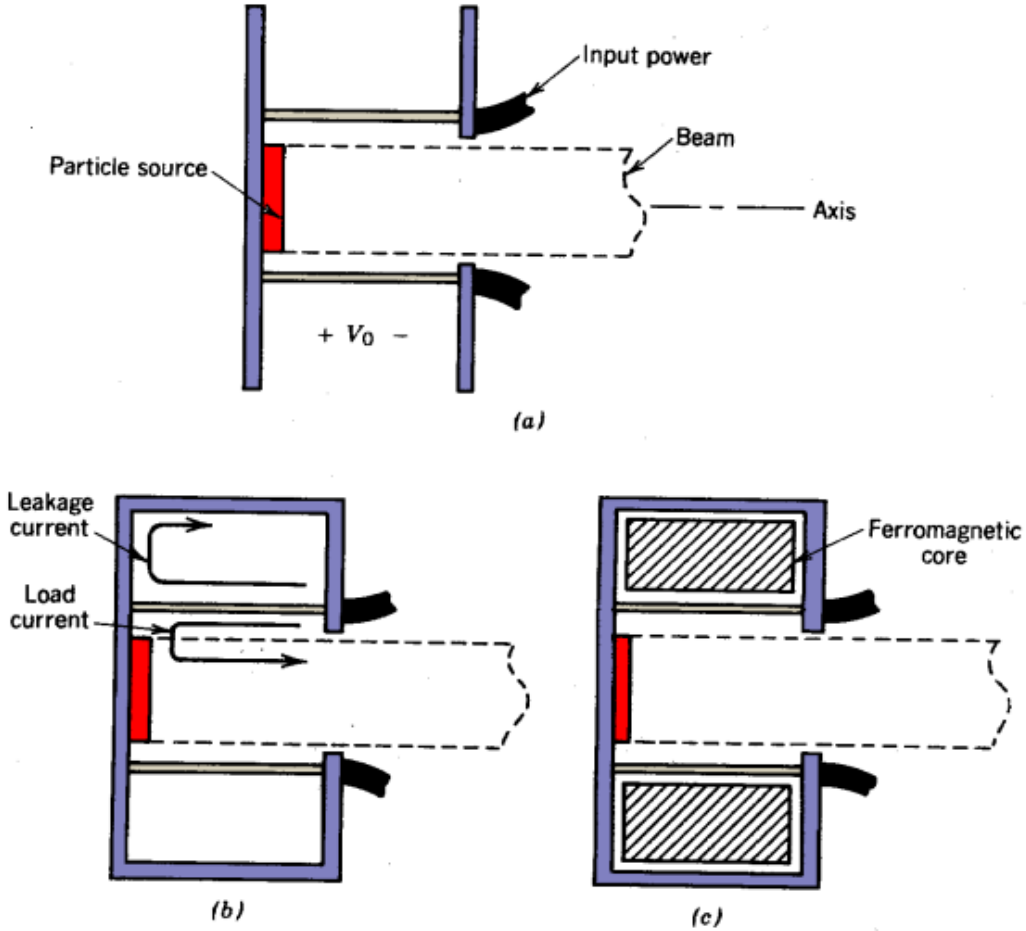
Course Outline

- Linear induction accelerators and inductive adders
- Impedance and propagation of adder structure
- Adder advantages/disadvantages
- Core considerations
- Examples of adders
- Minimizing rise time of adders
- Adder design example

Linear Induction Cavity

- An external voltage as shown is (a) is used to accelerate charged particles due to Lorentz force. Adding another accelerating structure to the right would require isolation of the voltage source.
- A cavity is created in (b), which is convenient for keeping the power supply at ground, but allows for high currents.
- A core is added to the cavity in (c) to create a large impedance to ground for high frequency or pulsed voltages to limit ground current.



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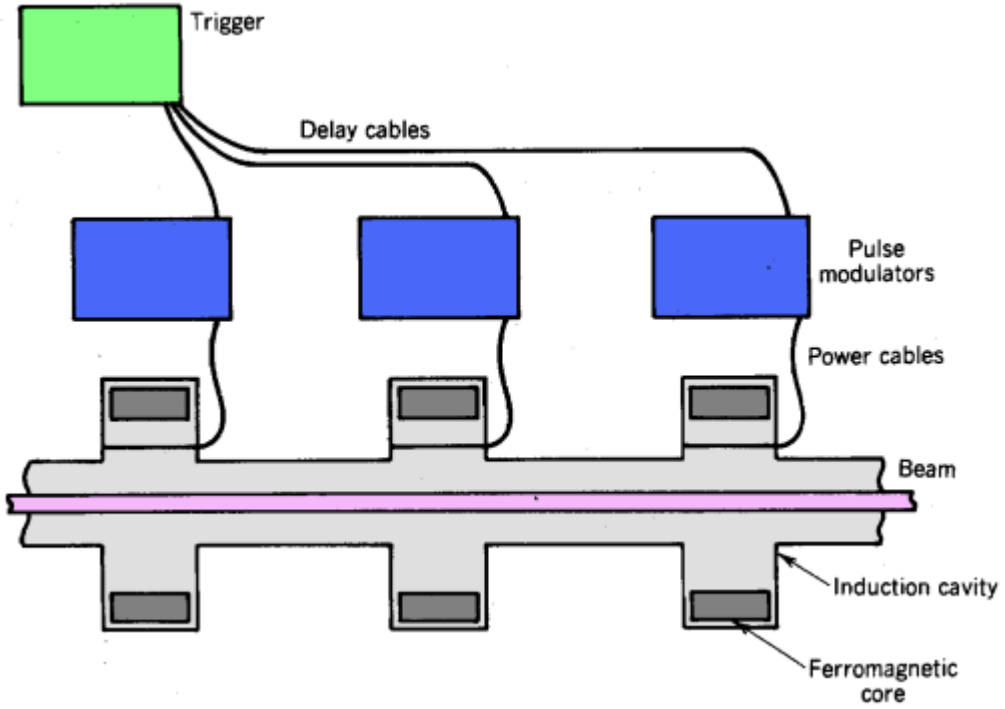
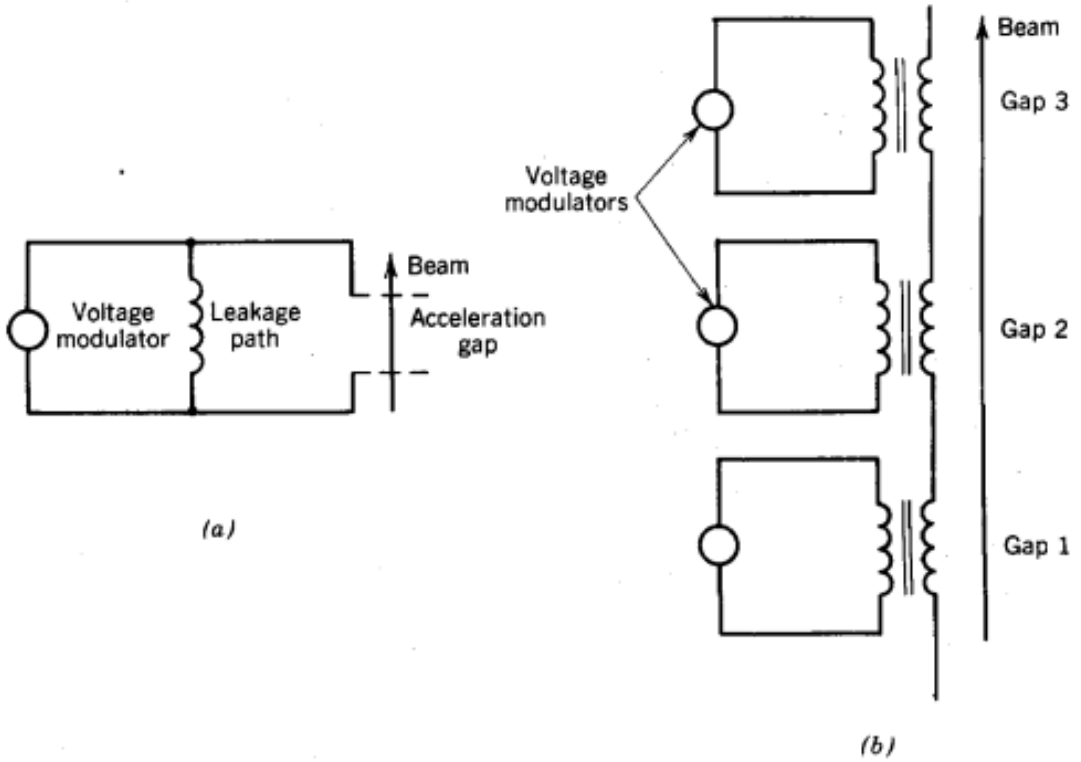
Linear Induction Accelerator



Three induction cells in a linear accelerator.

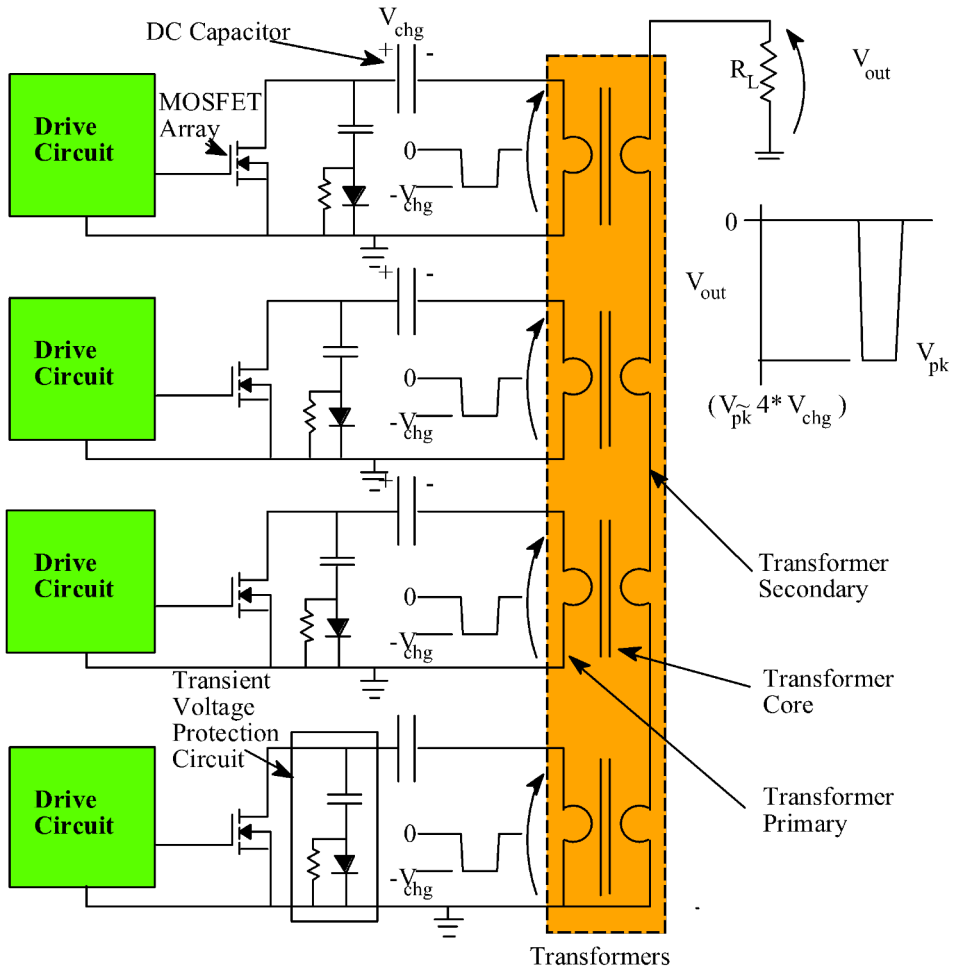


Equivalent circuit of a 3 cell induction linac.

*[1]

Solid State Inductive Adder

- Analogous to an induction linac but using a wire to pass through the cores to for a secondary winding of a transformer.
- N identical low (limited by switch) voltage modules
  - Hard tube
    - MOSFET
    - IGBT
  - Linear amplifier
- Each module drives a single-turn high bandwidth output transformer
- The transformer secondaries are connected in series to inductively add the voltage of the individual modules
- Modules remain at ground potential throughout the pulse



Impedance of Adder

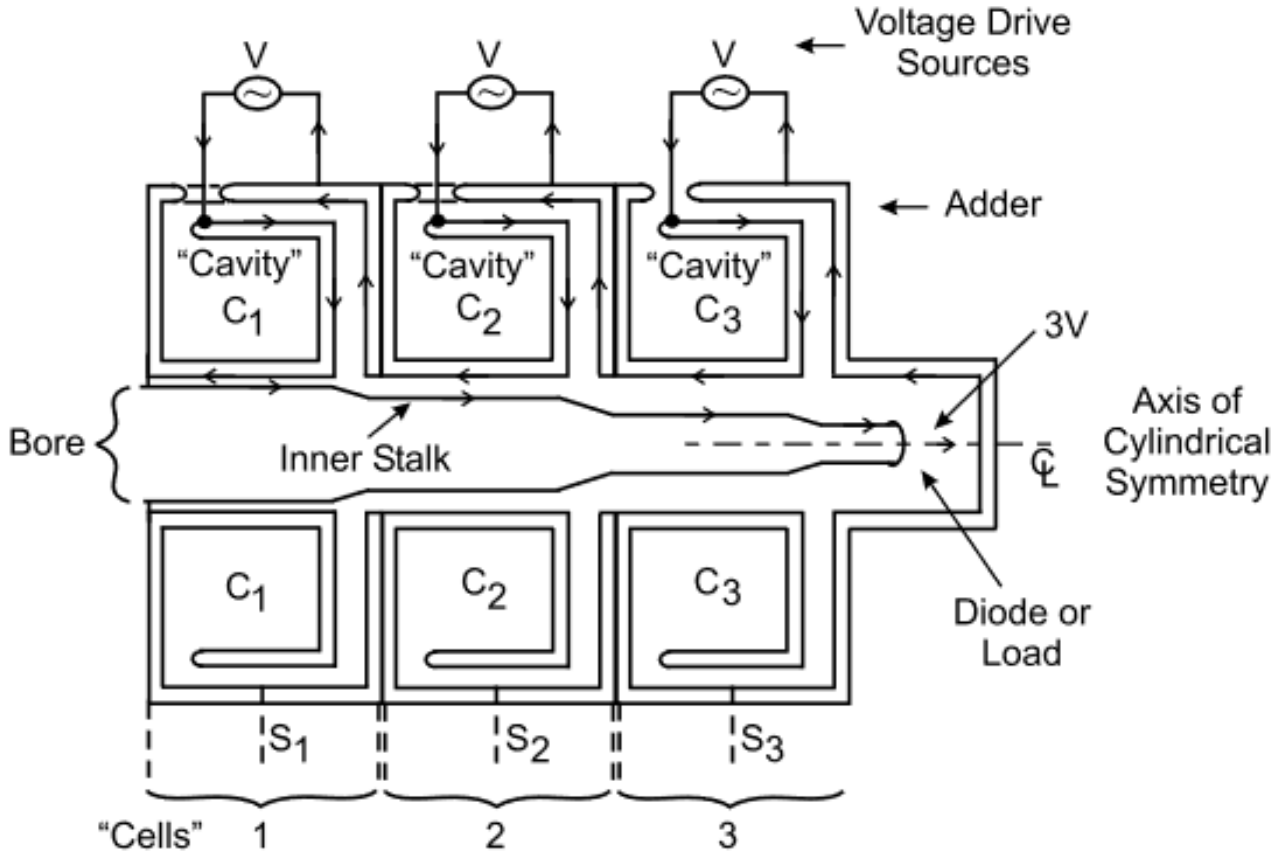
- The impedance of the structure can be calculated as:

$$Z_a = \sqrt{\frac{L_p + L_a}{C_a}}$$

$$L_a = \frac{\mu h}{2\pi} ln\left(\frac{b}{a}\right)$$

$$C_a = \frac{2\pi\varepsilon h}{ln\left(\frac{b}{a}\right)}$$

Lp is the primary inductance, h is the height of a cell, b is inner diameter of core housing and a is outer diameter of the secondary.



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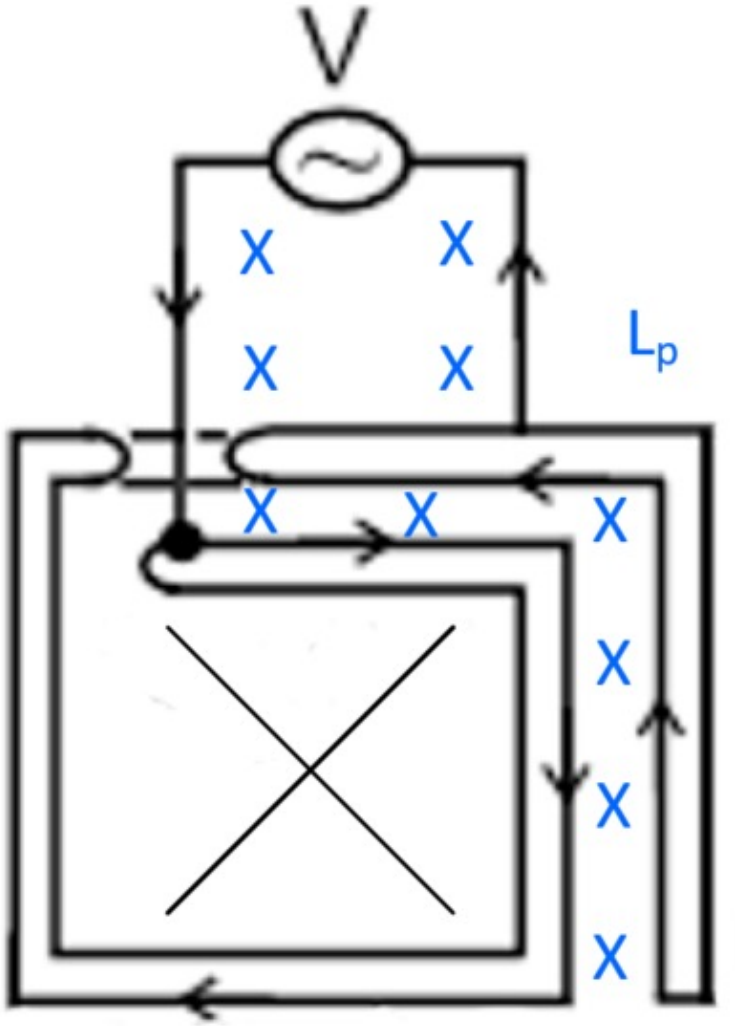
Propagation Time of Adder

- The propagation time for the structure is calculated by:

$$\tau \approx 2N \sqrt{L_p \frac{2\pi\varepsilon h}{ln\left(\frac{b}{a}\right)} + h^2 \mu\varepsilon}$$

The propagation time is dominated by the height of the adder structure. For fast rise time, use as short a cell height as possible to support the volt-seconds and droop requirement, a low value of dielectric constant, and minimize the primary inductance.



Inductive Adder Topology - Advantages

- All drive components ground referenced
- No high voltage grading required (except transformer secondary)
- Pulse format defined by programmable pulse generator
  - Pulse width agility
  - Burst frequency agility
  - High burst frequency >1 MHz
- Modular - adder consists of stack of identical modules
  - All modules switch same voltage/current
  - All modules triggered simultaneously
  - Scaleable to higher voltages by adding modules
- Low source impedance
  - Can drive wide range of load impedances
  - Load voltage is essentially independent of load

Inductive Adder Topology - Issues

- Each module must switch full load current
  - May require many parallel components (switches, capacitors, etc.)
  - Parallel switching devices must have low jitter on both turn-on and turn-off
- Requires very low inductance in primary circuit
- Requires very fast opening switch that can interrupt full load current and survive fault currents
- Fault currents can be very large, especially if cores saturate
- Cost
- Complexity

Inductive Adder Design Considerations

- Select Switch and switch drive circuit
  - Switching speed for both turn-on and turn-off
  - Maximum operating voltage (determines number of modules)
  - Current Rating (determines number of parallel devices)
- Size the capacitor (bank)
  - Must be large enough to meet droop requirements
  - Inductance must be low
  - Low ESR (equivalent series resistance)
- Design the pulse transformer
  - Use high frequency core material
  - Core area must be sufficient for application
    - Total volt-seconds for single pulse if reset between pulses
    - Total volt-seconds for all pulses in burst if reset between bursts

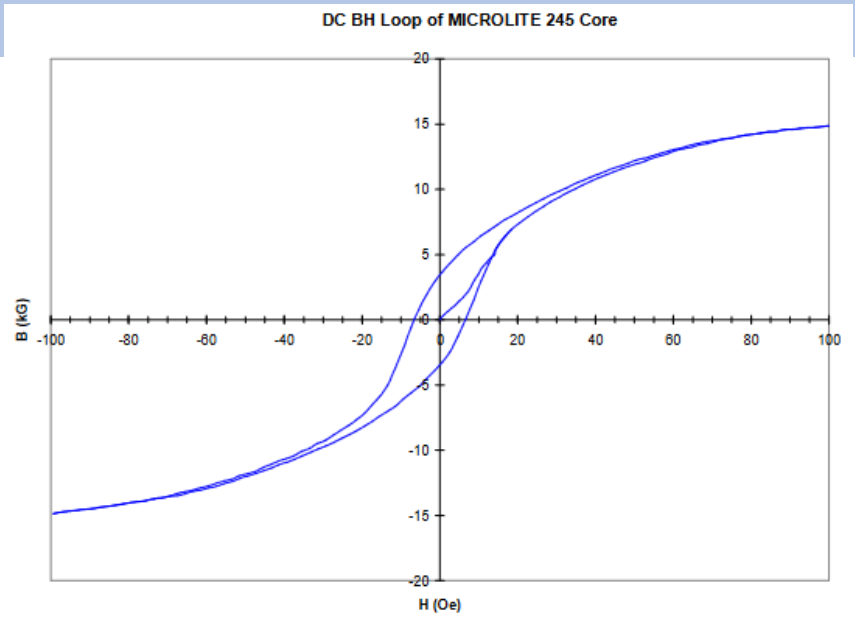
Inductive Adder Design Considerations

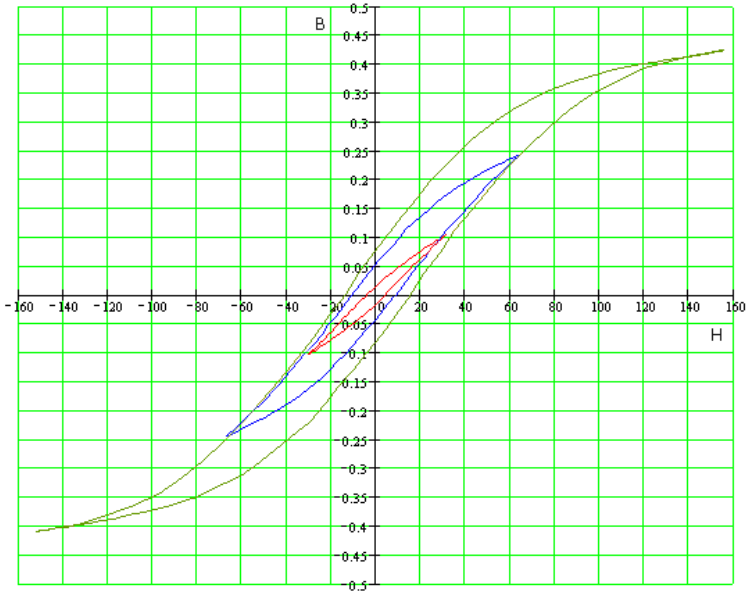
- Make sure that primary circuit inductance is minimized
  - Voltage drop across loop inductance during high di/dt affects load voltage
  - Energy stored in loop inductance can appear as voltage across switch
  - Consider component inductances, transformer leakage inductance, and inductance of circuit board traces
- Protection circuits for switches
  - Overvoltage from $(L\ dI/dt)_{primary}$ on turn off
  - Overcurrent; load faults, transformer saturation
- Reset of adder magnetic core
  - Duty cycle sets minimum ratio for V_{reset}/V_{output} (total $V\tau = 0$)
- Recharge of capacitor between pulses/bursts
  - Interpulse recharge can reset core if voltage and current high enough

Magnet Core Hysteresis

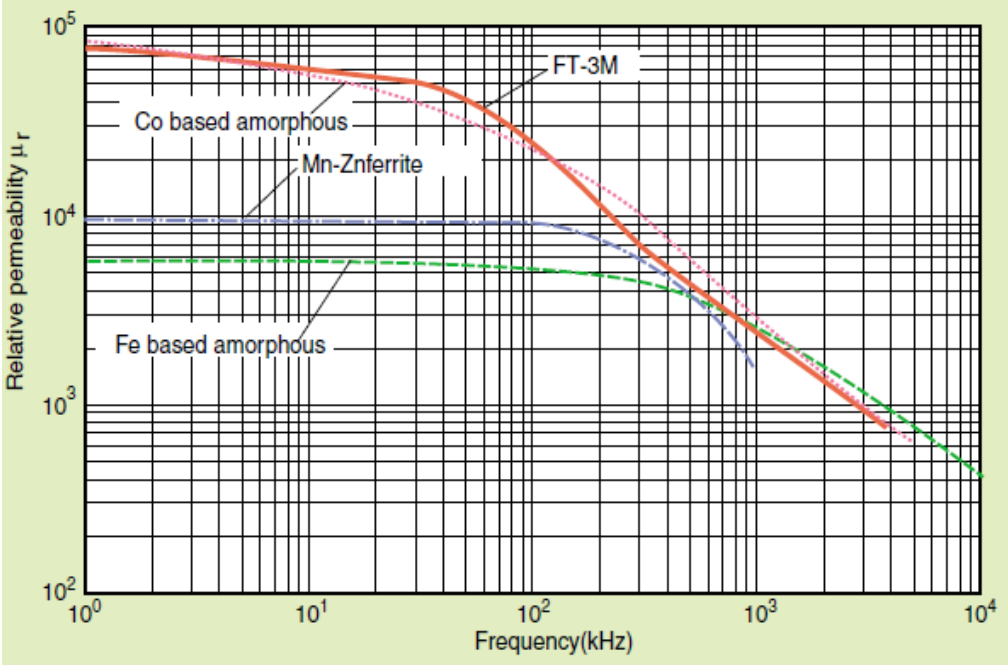
- For ferromagnetic materials, the relative permeability μ_r is not linear, $\boldsymbol{B} = \mu_r \mu_0 \mathbf{H}$.
- Relative permeability varies with magnetic field, frequency and temperature and reaches saturation where the magnetization of the core does not increase further with applied field, ~15 kG for the core at right.
- You may see it plotted as volt-seconds vs Ampere.

*[2]





Relative Permeability



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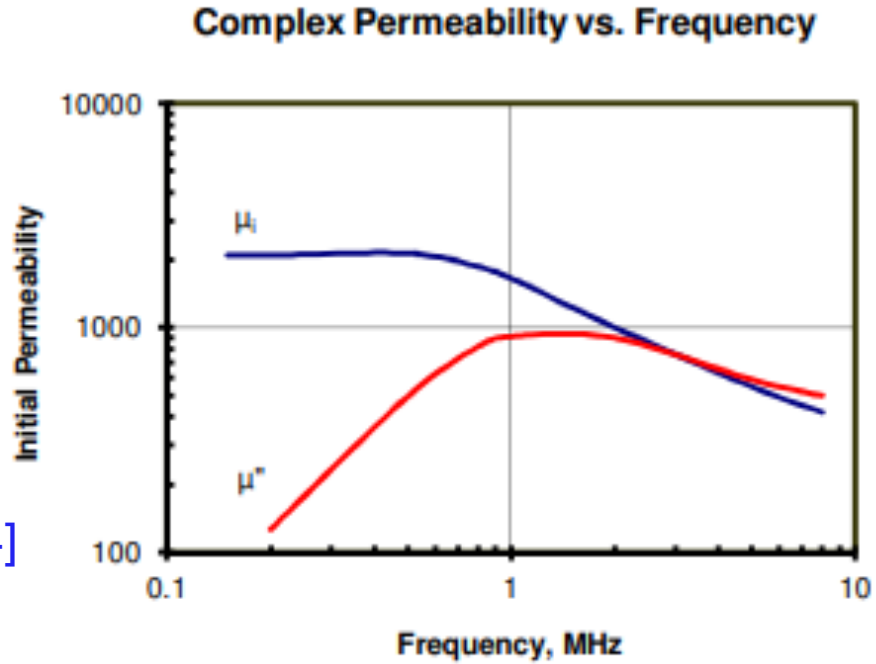
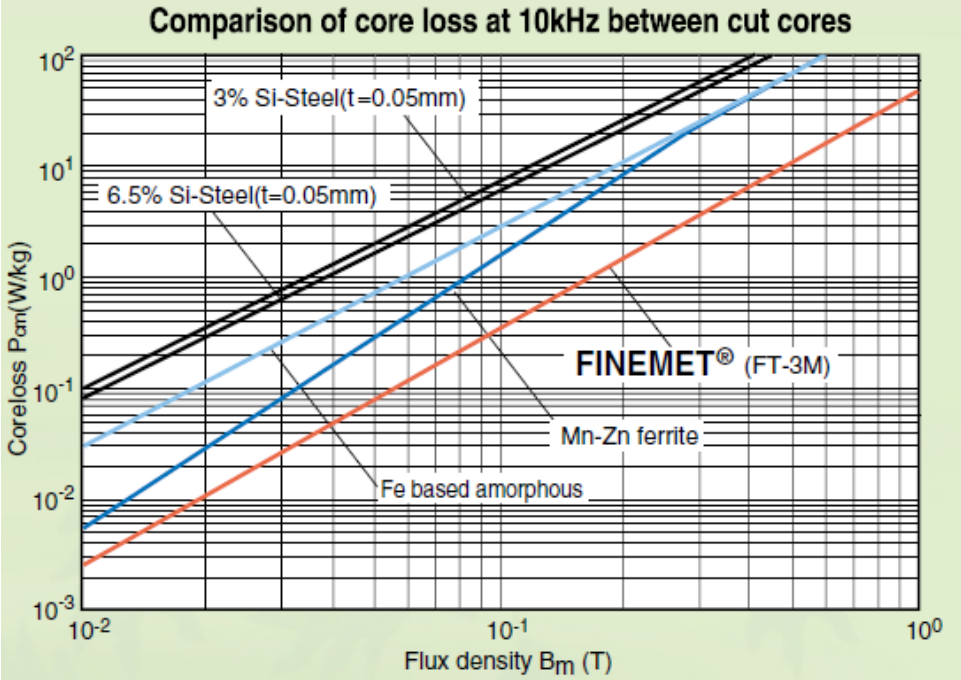


*[4]

- Relative permeability drops with increasing frequencies and is a function of the core material used.
- Iron based cores generally have higher initial permeability than ferrite cores.
- Ferrite cores generally support higher frequencies before rolling off.

Core Loss

- Core loss is given as W/kg, and is dependent on frequency, flux swing and temperature.
- All should be considered in the design of an adder, especially at high pulse rates.



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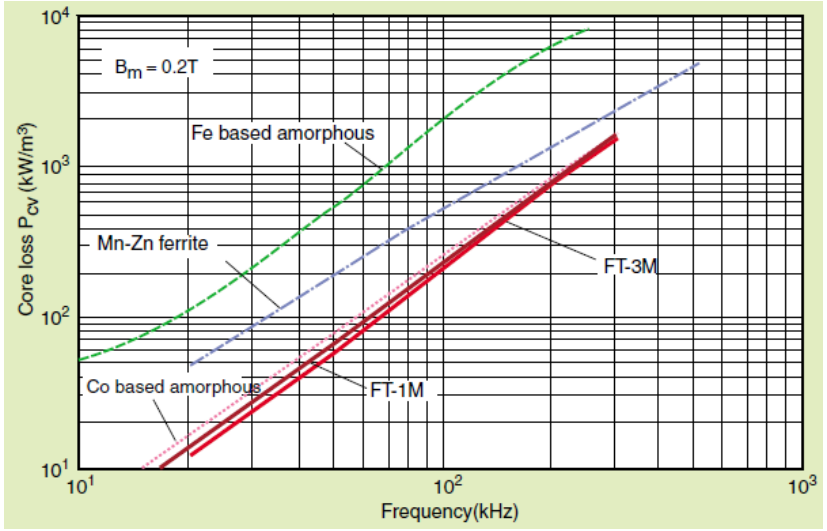
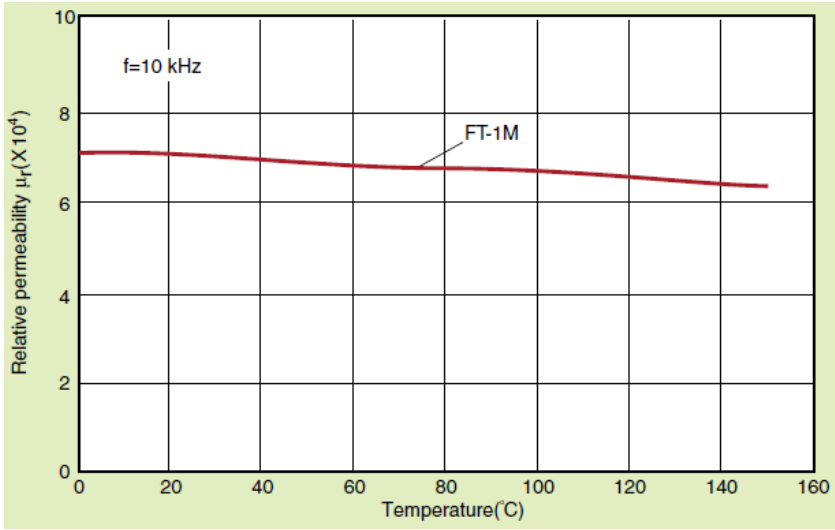
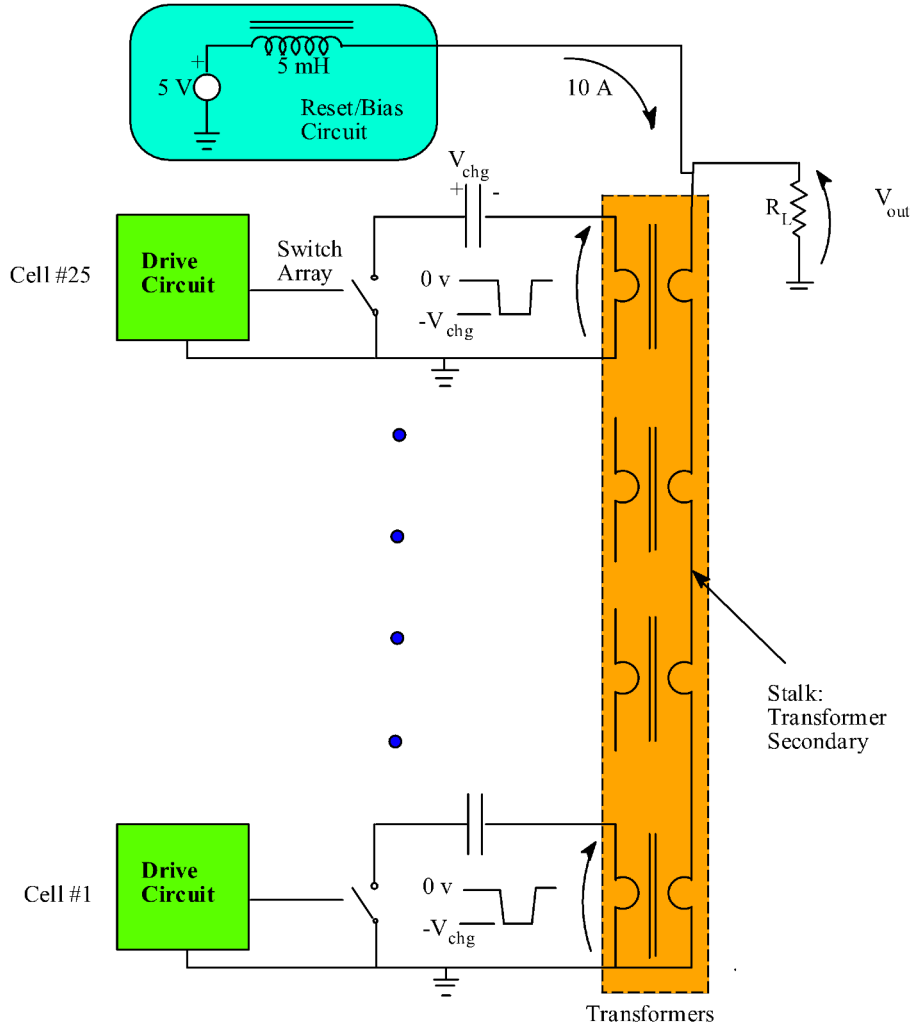




Core Reset/Bias Circuit

- Voltage induced into the primary resets the magnetic core material between bursts
- H-field created by the DC current biases the magnetic cores to a single point on the BH curve.
- Reset through the secondary winding resets all the cores
- The series inductor protects and isolates the reset power supply from the high voltage output pulse
- Other reset circuits can be used: DC reset through the primary, pulsed current into either the primary or secondary

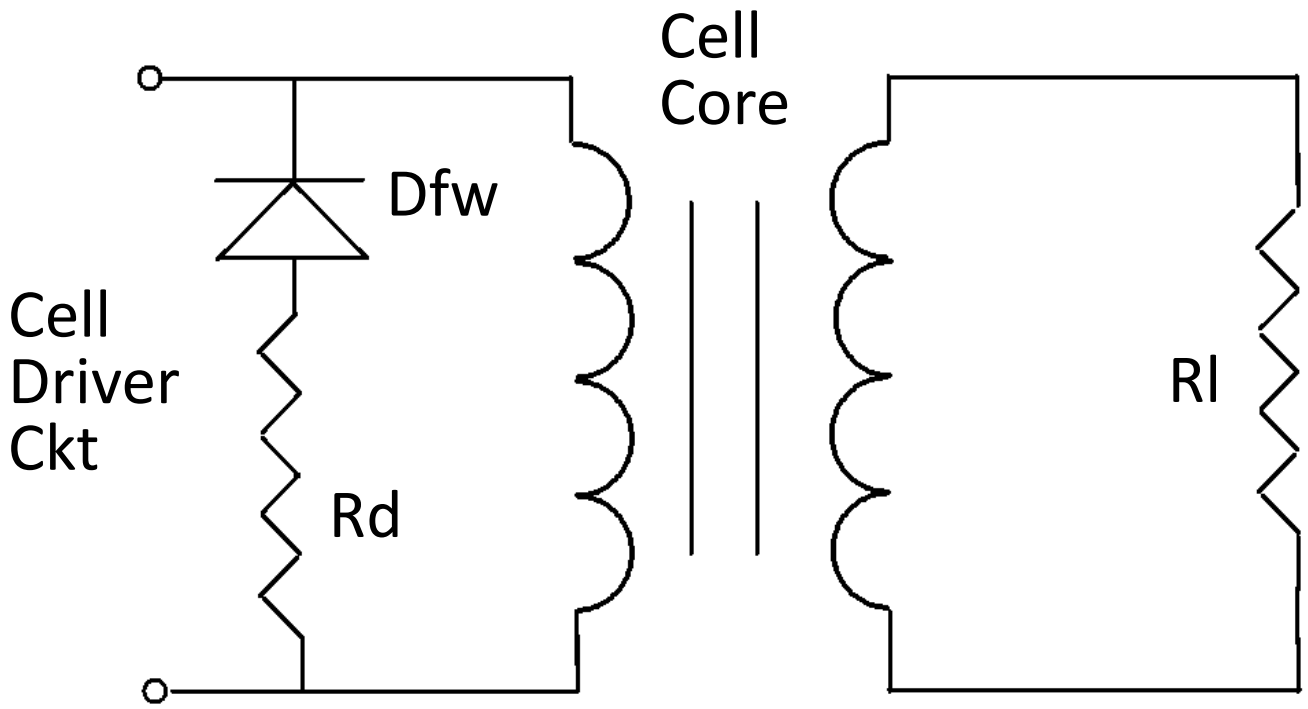


Core Magnetizing Inductance

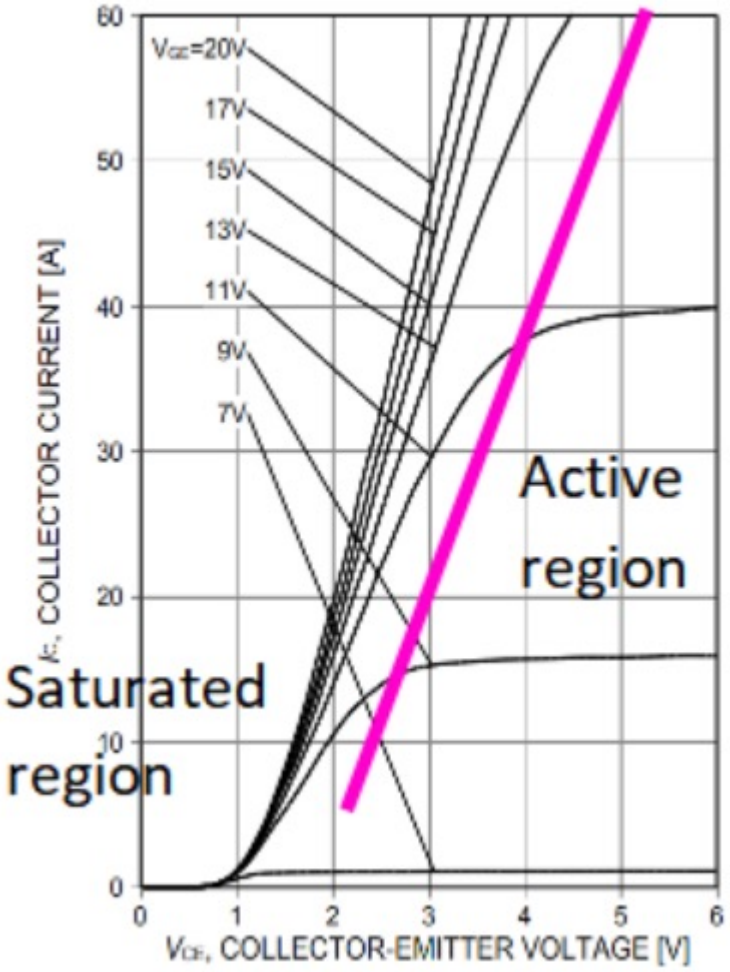
An inductive voltage spike at the end of the pulse can damage the switch.

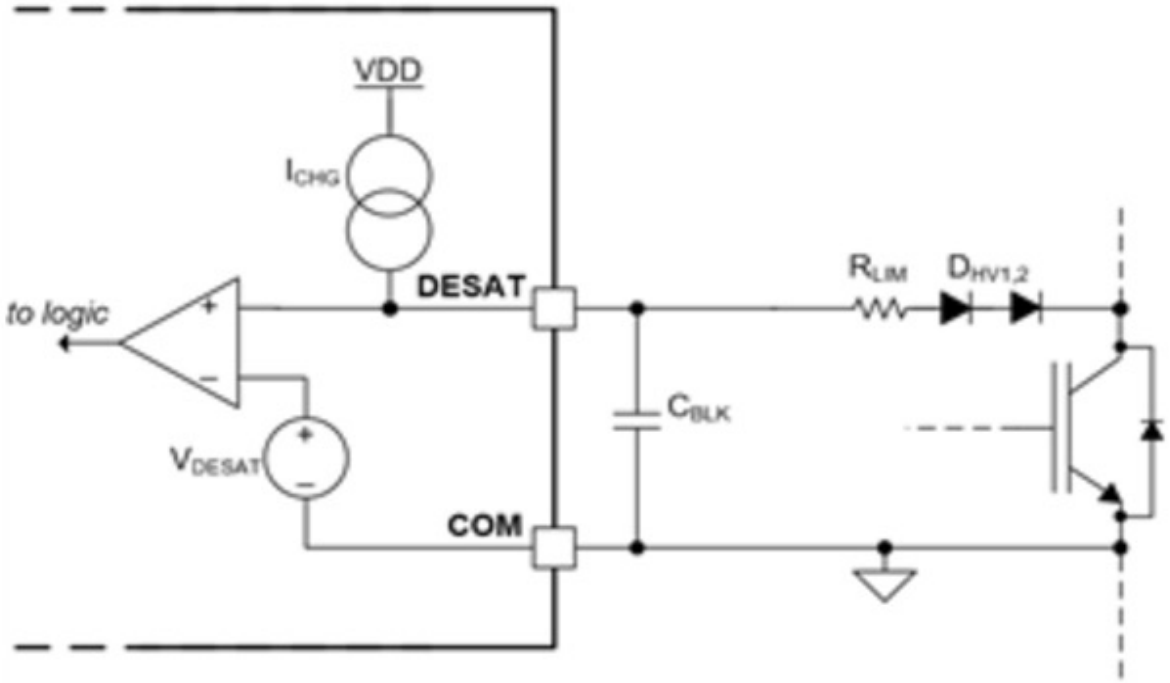
Adding a freewheel diode across the primary protects the switch, but allows magnetizing current to circulate in the primary.

You may need to add a resistor in series with the diode for fast turn off.



Short Circuit Protection





IGBTs operating in the active region have high losses. For pulses > 1 µs long, you need to protect the switch from short circuits at the load. Core saturation is particularly damaging. Use a de-saturation protection circuit and drive the IGBT at the lowest voltage possible to meet the current and rise times requirements.

Example 1 - NLC Solid-State Modulator

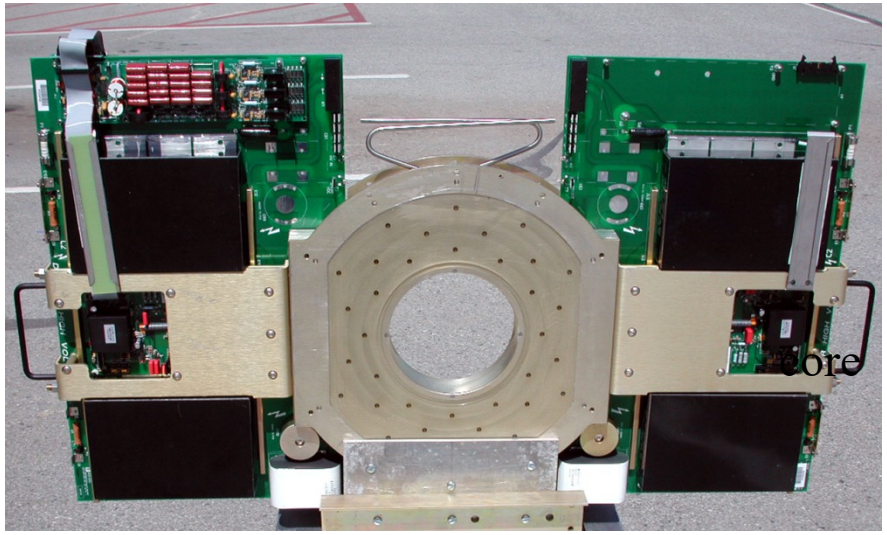
- Why use inductive adder
  - 2 TeV center of mass collider using 2000 klystrons, for comparison SLC was 100 GeV center of mass with 200 klystrons and operated at about 50 MW average power.
  - Would need a dedicated power plant to provide power and a maintenance crew of 100s based on SLAC experience and scaling.
  - SS inductive adders offered improvements in cost, efficiency and maintainability over PFN/thyratron modulators.
- Modulator Requirements:
  - Output Voltage 500kV @ 2kA
  - Pulse-width - 3µs
  - Klystron Efficiency > 80% (rise & fall times less than 400 ns)
  - Repetition Rate - 120 Hz (500kW Average)
  - Lifetime - 30 years
  - Cost < 200k$/ Modulator
  - Each modulator drives 8 klystrons

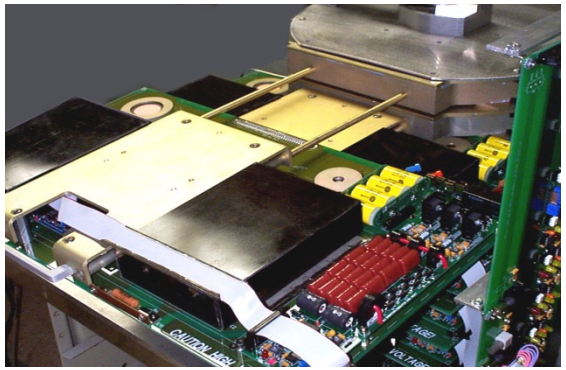
Example 1 - NLC Modulator

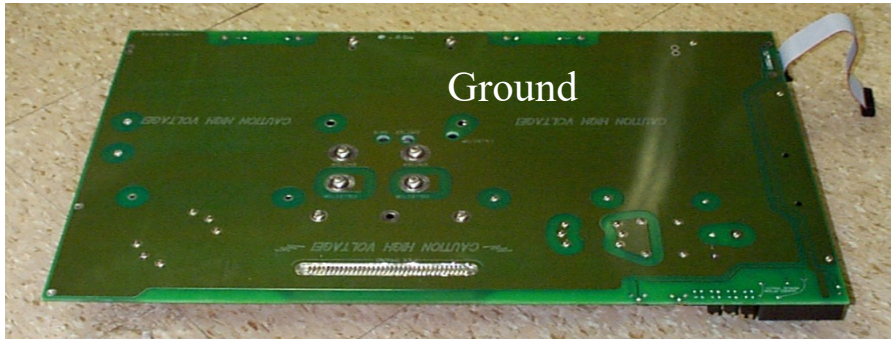
- FRACTIONAL TURN PULSE TRANSFORMER
  - MULTIPLE PRIMARIES ONE END GROUNDED
    - 76 Primaries with 3 turn Secondary
    - Primary uses low losses Metglas (or Finemet) cores
  - SECONDARY CONNECTED IN SERIES
  - 500 kV @ 2080 A, 1040 Meg watts for 4 μs at 120 Hz, 500 kW Average uses solid-state IGBT driver
  - **IGBTs** ARE BIPOLAR TRANSISTOR WITH FET INPUT GATE
  - 152 IGBT's (two per Primary)
  - 3200 Amps, 4 μs pulses each IGBT
  - 2200 volts per IGBT rated at 3.3 kV-800 A

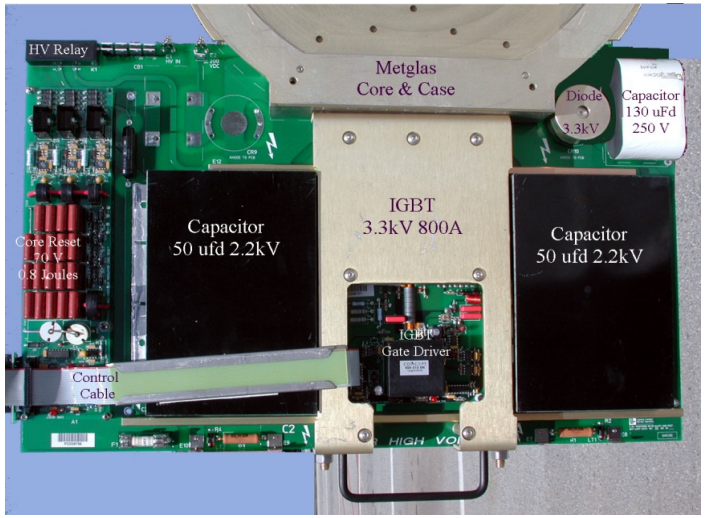
- MAJOR CONCERNS
  - Klystron protection when there are internal faults (limit energy in klystron arcs)
  - IGBT protection when load faults (requires active sense and control circuitry)

NLC - IGBT Drivers and Core



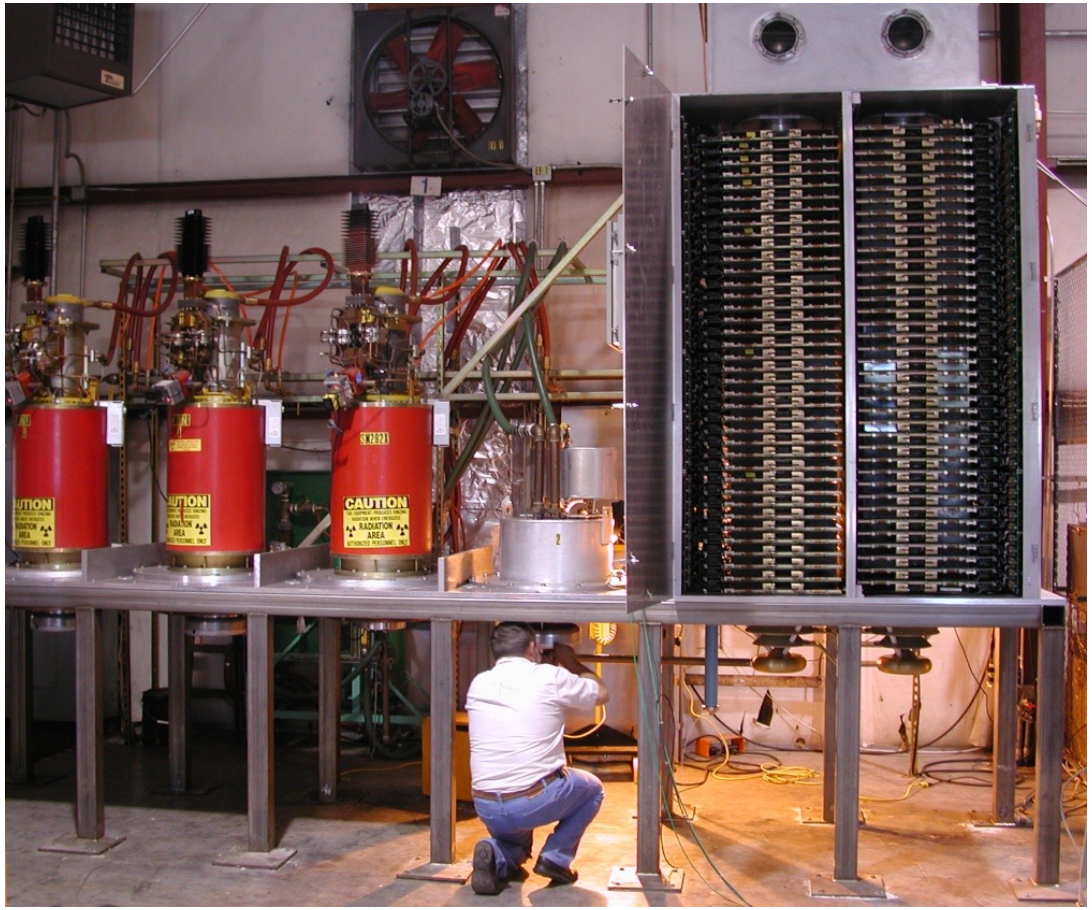




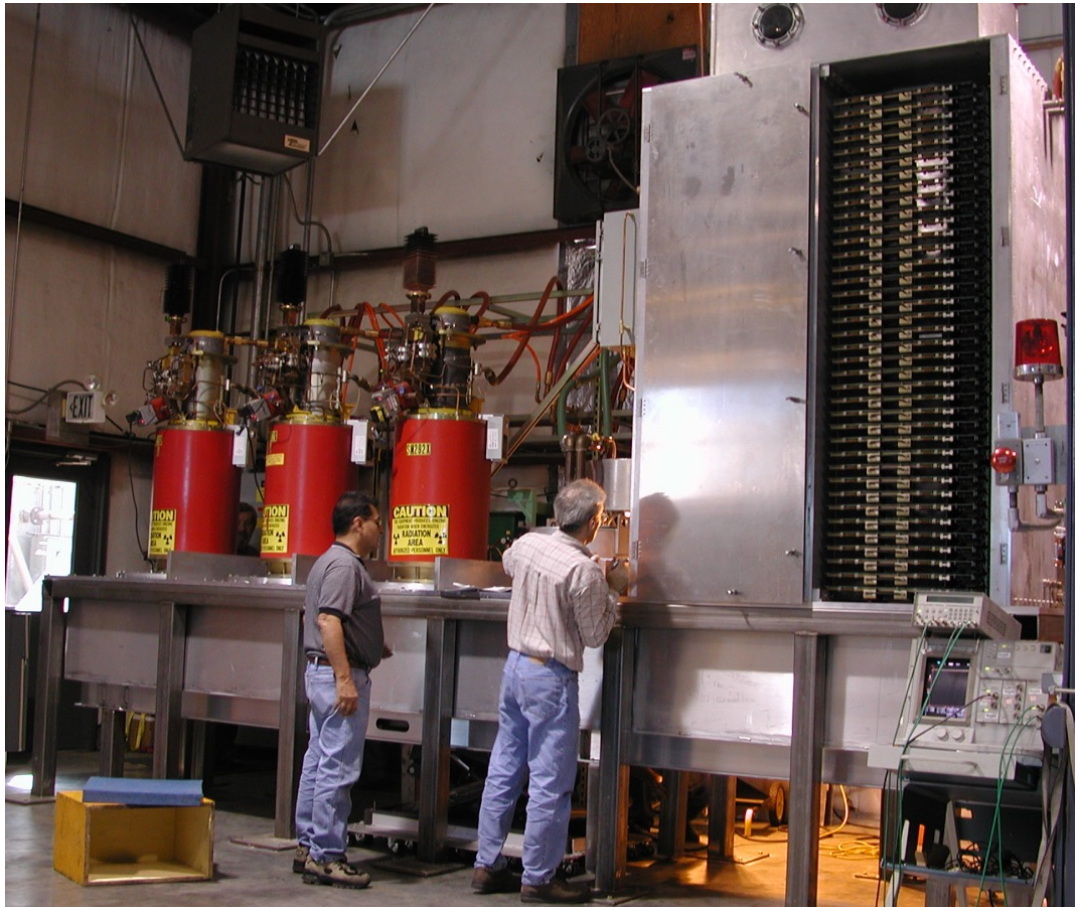


First prototype used two parallel, 3.3 kV IGBTs driving a METGLAS core. The cores were reset between pulses. A freewheeling diode is used to bypass cells allowing rise time/flat top shaping.

Prototype NLC Solid State Induction Modulator



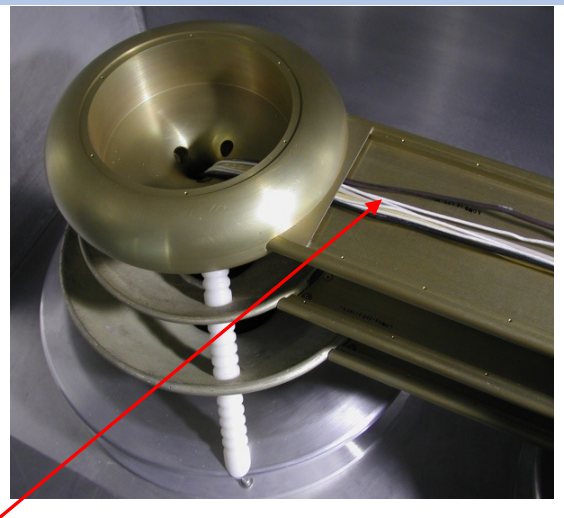
3 turn Secondary with 3 S-band klystrons and a water load installed

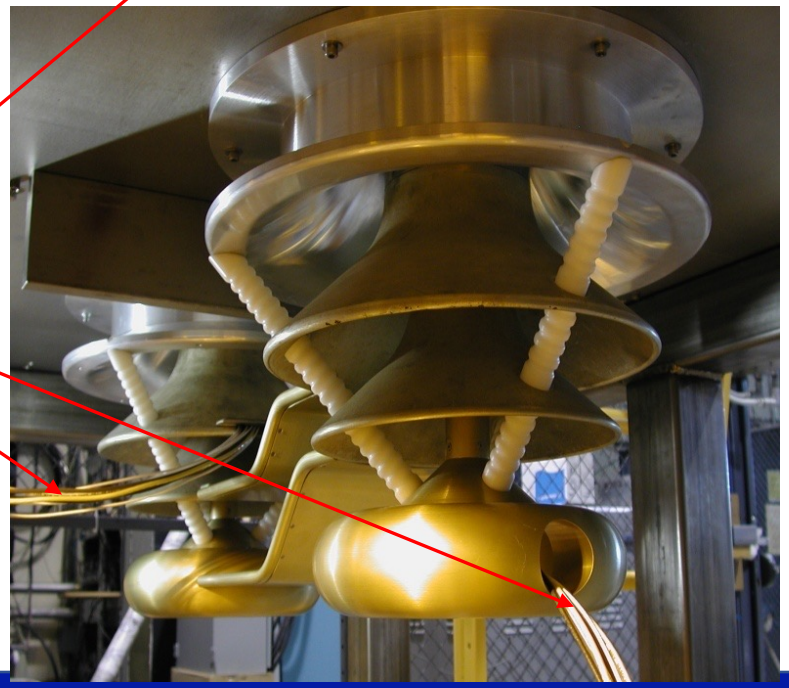


With HV oil tank installed

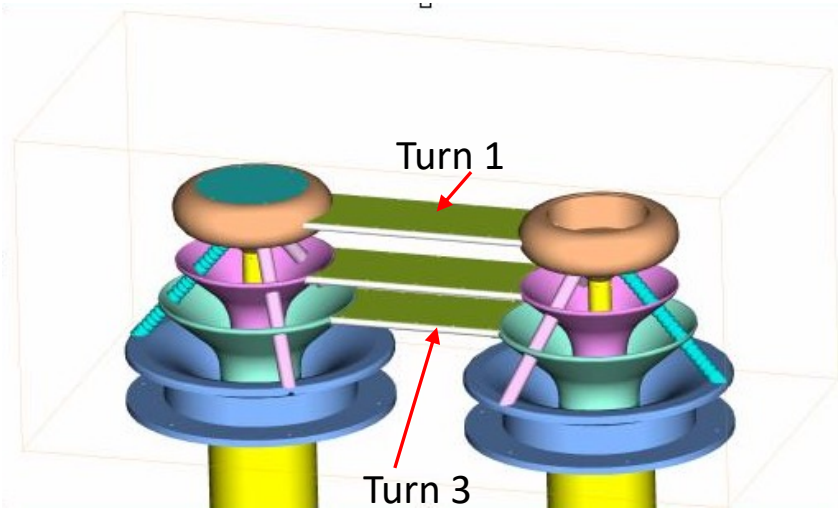
Prototype NLC Secondary Structure

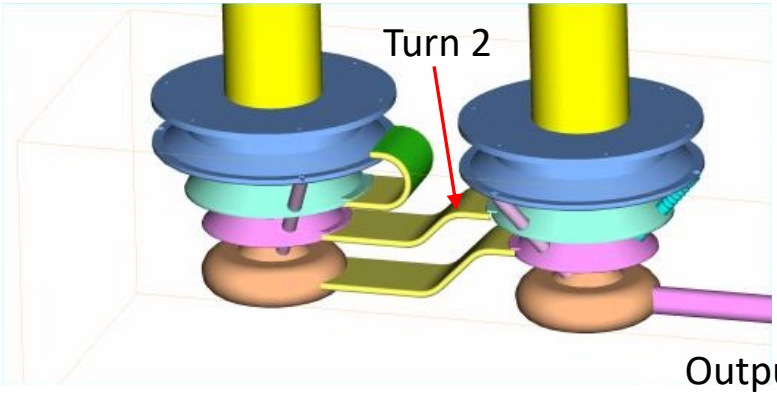
Coaxial Nested Three Turn Secondary End Connection





Klystron heater cables





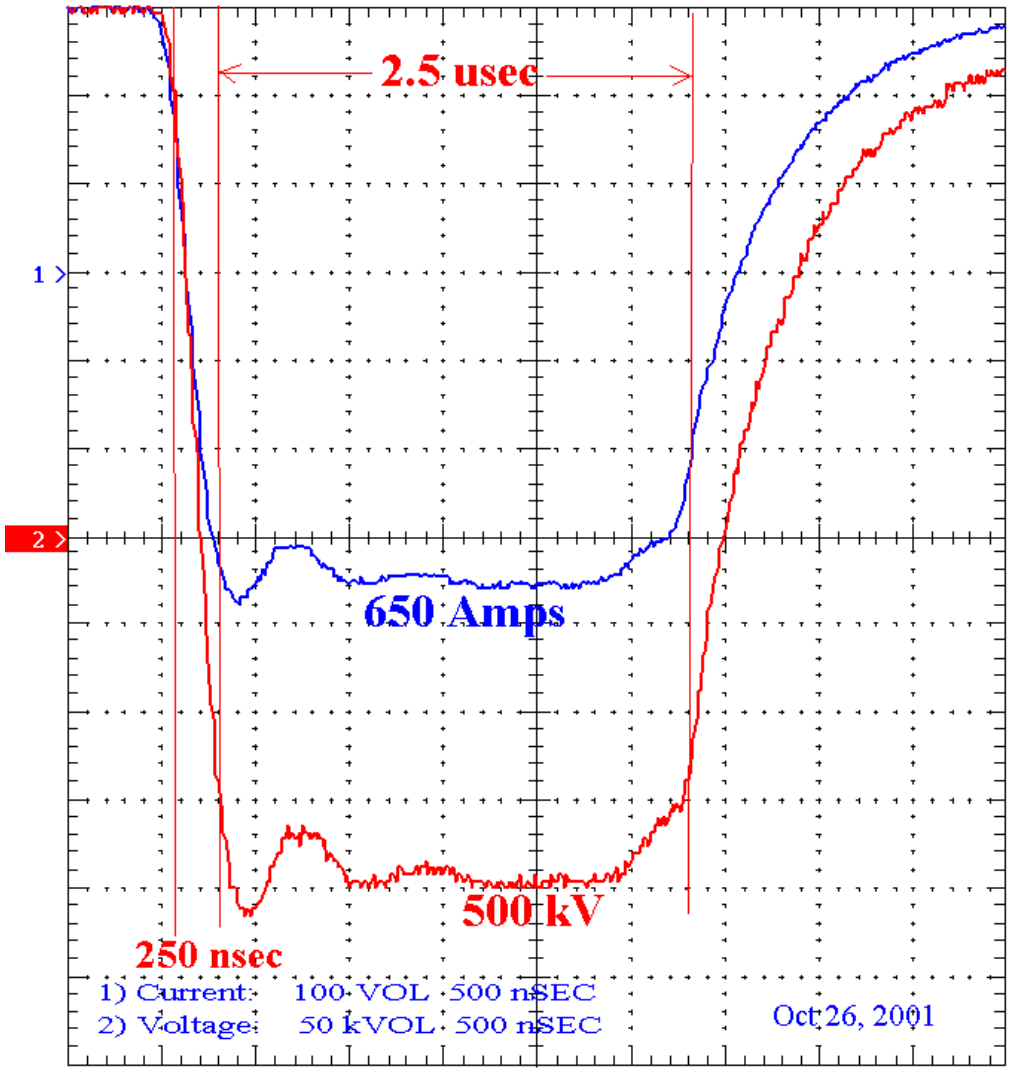
Output connector to 8 klystrons

Prototype NLC Modulator - Water Load

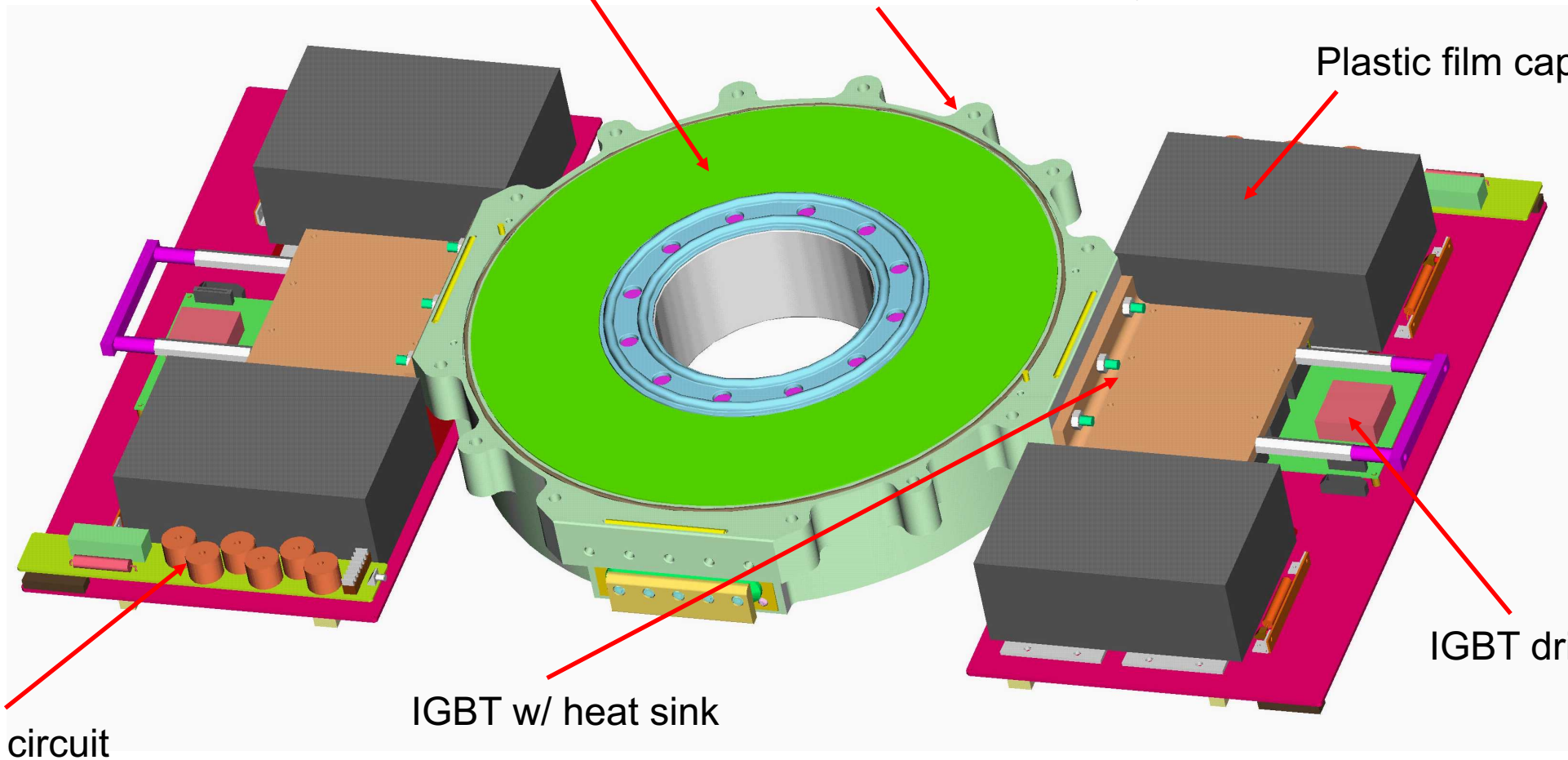
Three Turn Secondary

76 Metglas cores

152 IGBT Drivers



NLC Adder Cell w/Drive Boards (with 6.5kV IGBTs)



Comparison: Voltage Pulse of Induction Modulator vs. PFN

350 kV, 3.0 usec

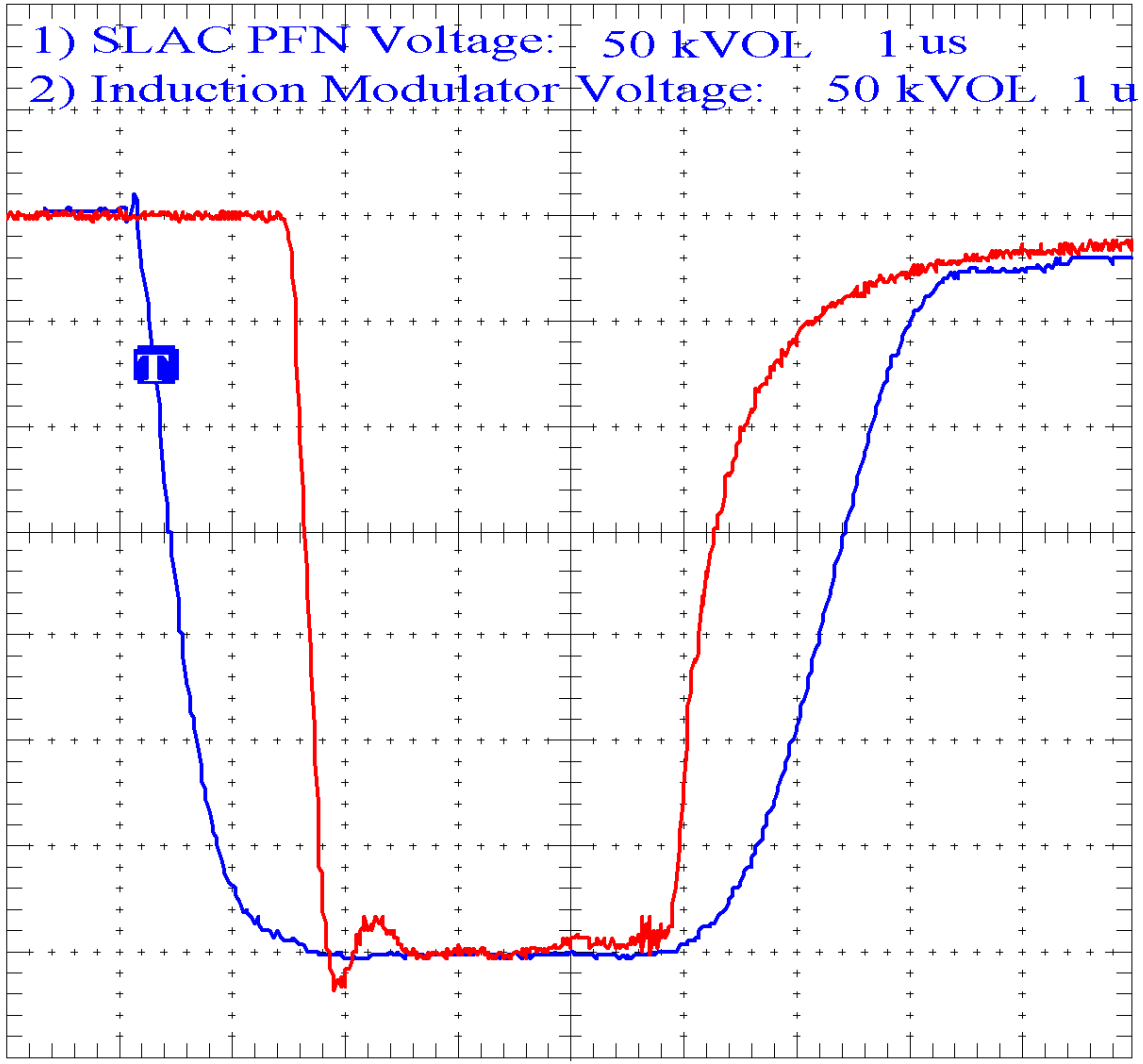
375 Amps PFN

750 amps Induction

Modulator waveform

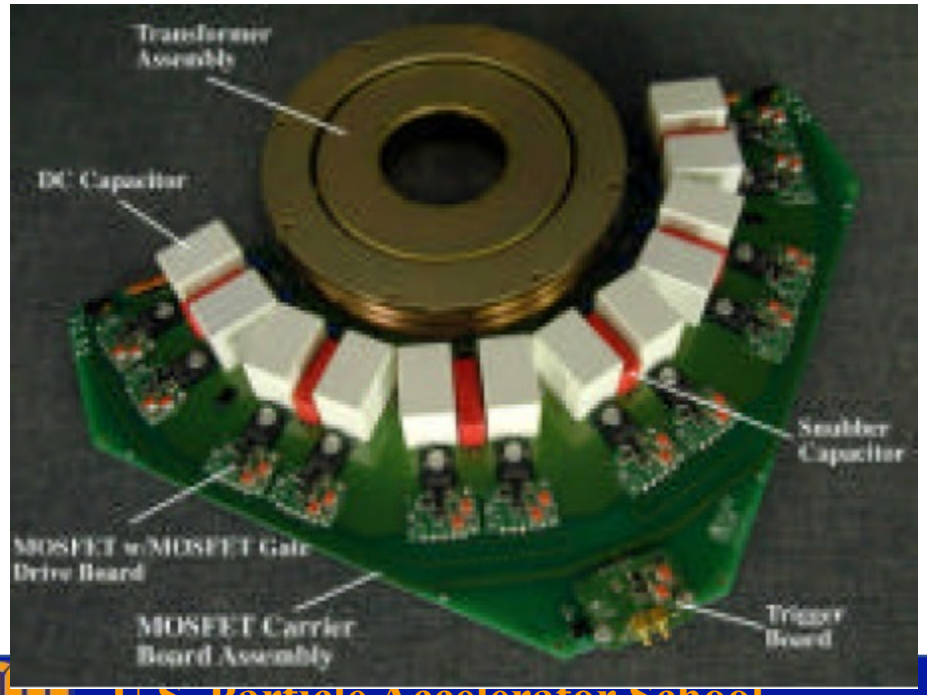
efficiency ~89%

Overall efficiency >80%



Example 2 – Darht-2 Kicker Modulator

Parameter	Requirement
Output Voltage	±20kV into 50Ω
Voltage Rise/Falltime	≤10ns (10-90%)
Flattop Pulsewidth	16ns–200ns (continuously adjustable)
Burst Rate	4 pulses @1.6MHz(~600ns between leading edges)



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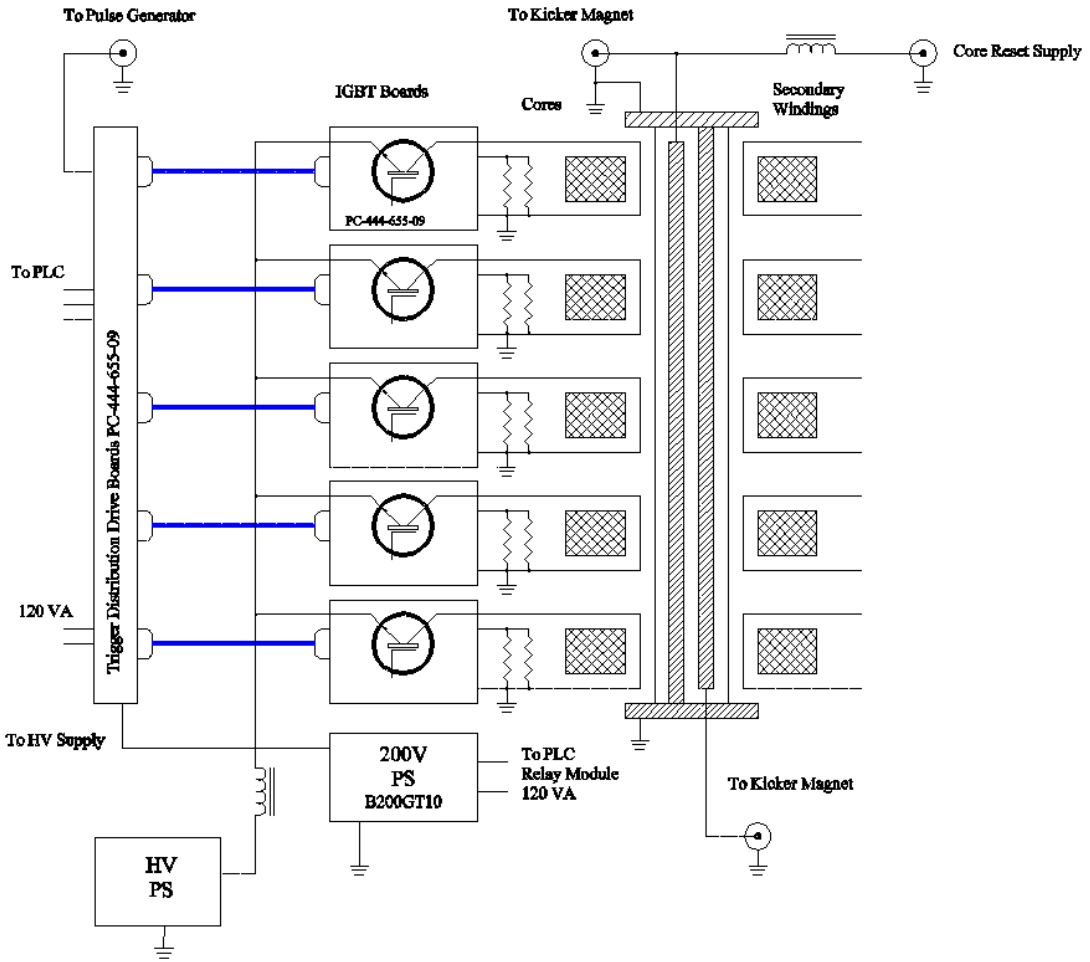
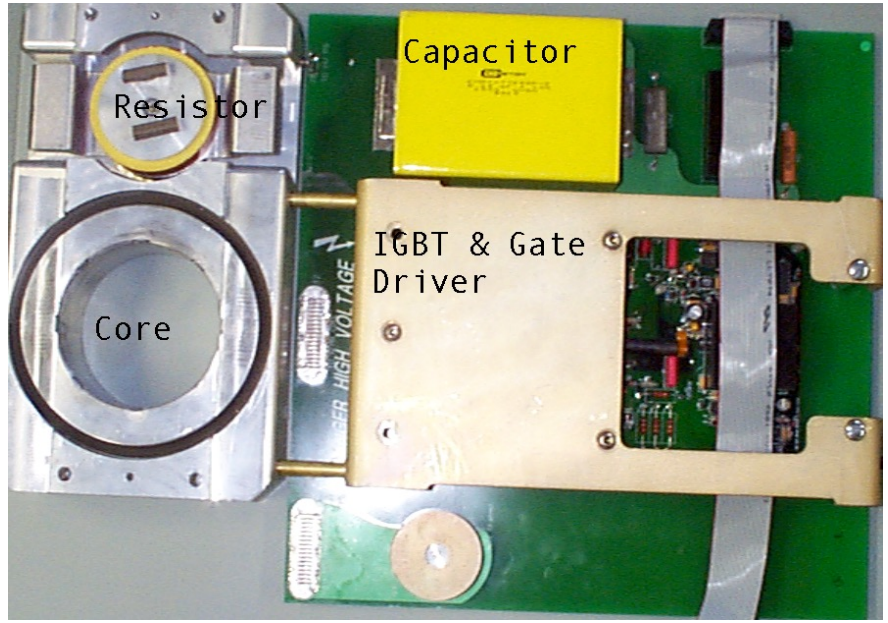
Bi-polar Induction Adders

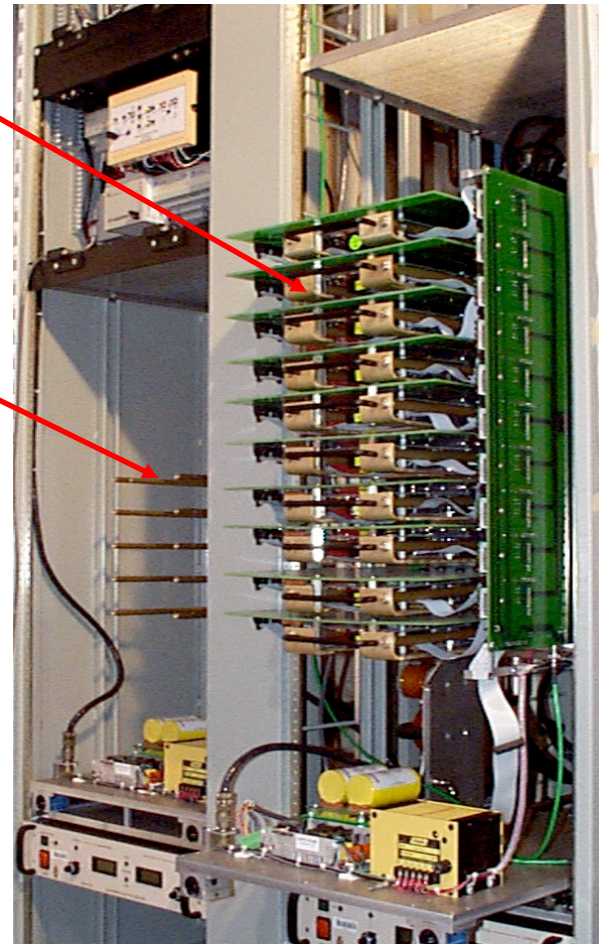
- Using two secondaries wound in opposite directions make for a bi-polar adder as shown.
- Five cells, each with a single turn primary and bi-polar single turn secondaries.
- Pulses are nearly identical.
- Good choice for driving pulsed magnets (stripline).



Spear 3 Kicker Modulator

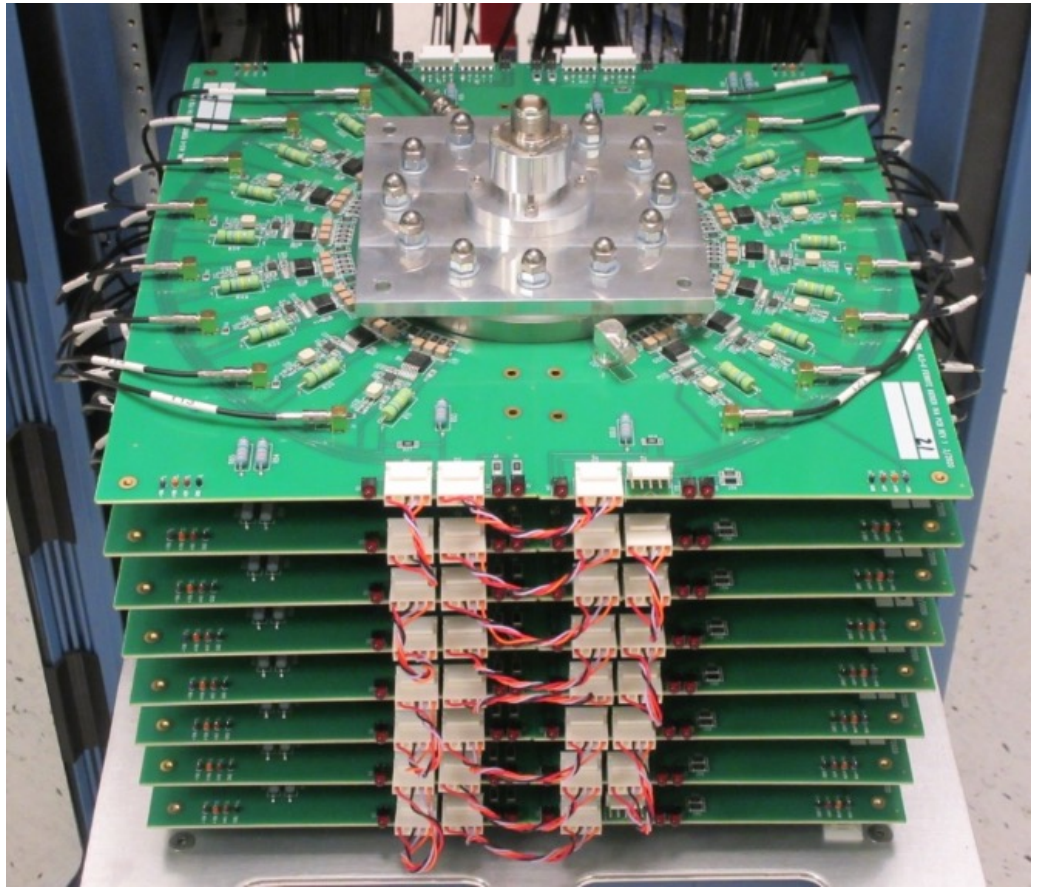
- ±10 kV and ±20 kV, depending on magnet
- 2620A and 2380 A, depending on magnet
- Five and ten cells, depending on magnet
- 375 ns rise time/fall time
- 750 ns pulse width





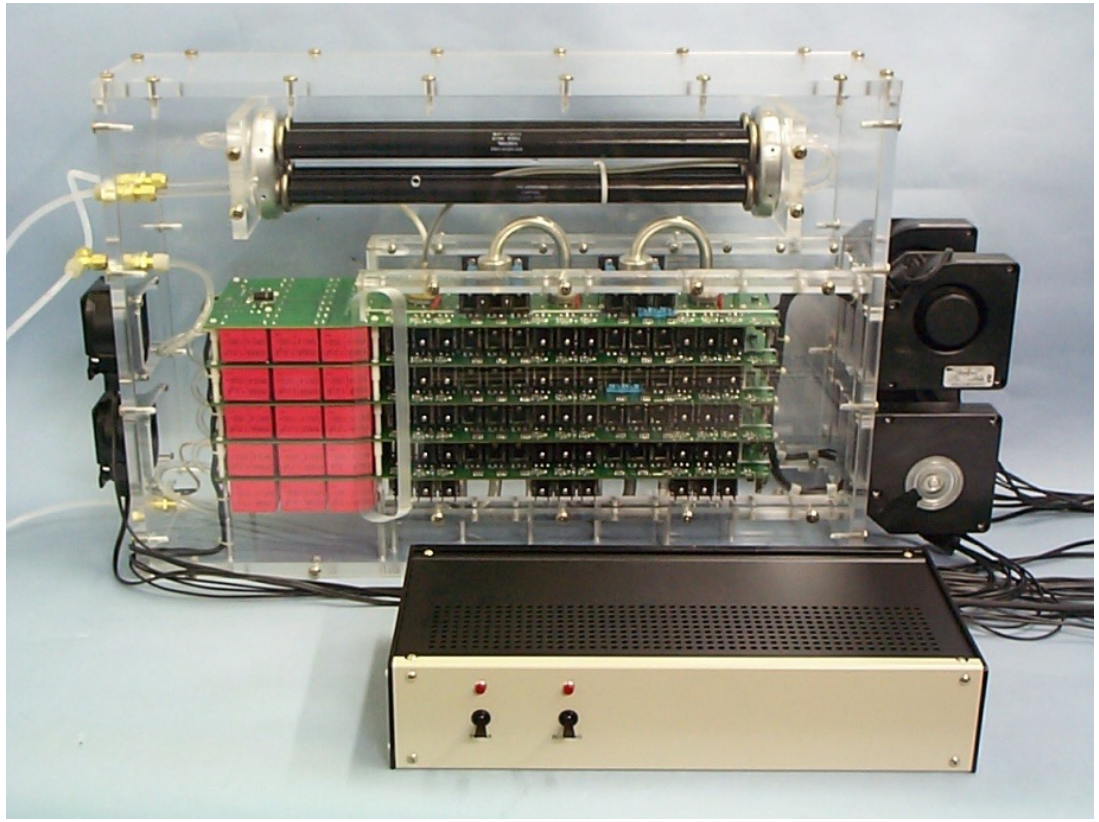
ALS-U Kicker Modulator

- Eight cell bipolar adder
- Vo = ± 5300 V into 50 Ω
- Rise fall times < 10 ns.
- Uses 16 parallel MOSFETs per cell.
- Adder structure is designed to be 25 Ω.
- Triggering can be adjusted for each MOSFET to compensate for variations in gate capacitance and optimize rise time.



Commercial Inductive Adder Modulator

- 20 kV
- 100A
- 100 ns pulse, ~15 ns rise/fall
- To 25 kHz
- To 3 kW

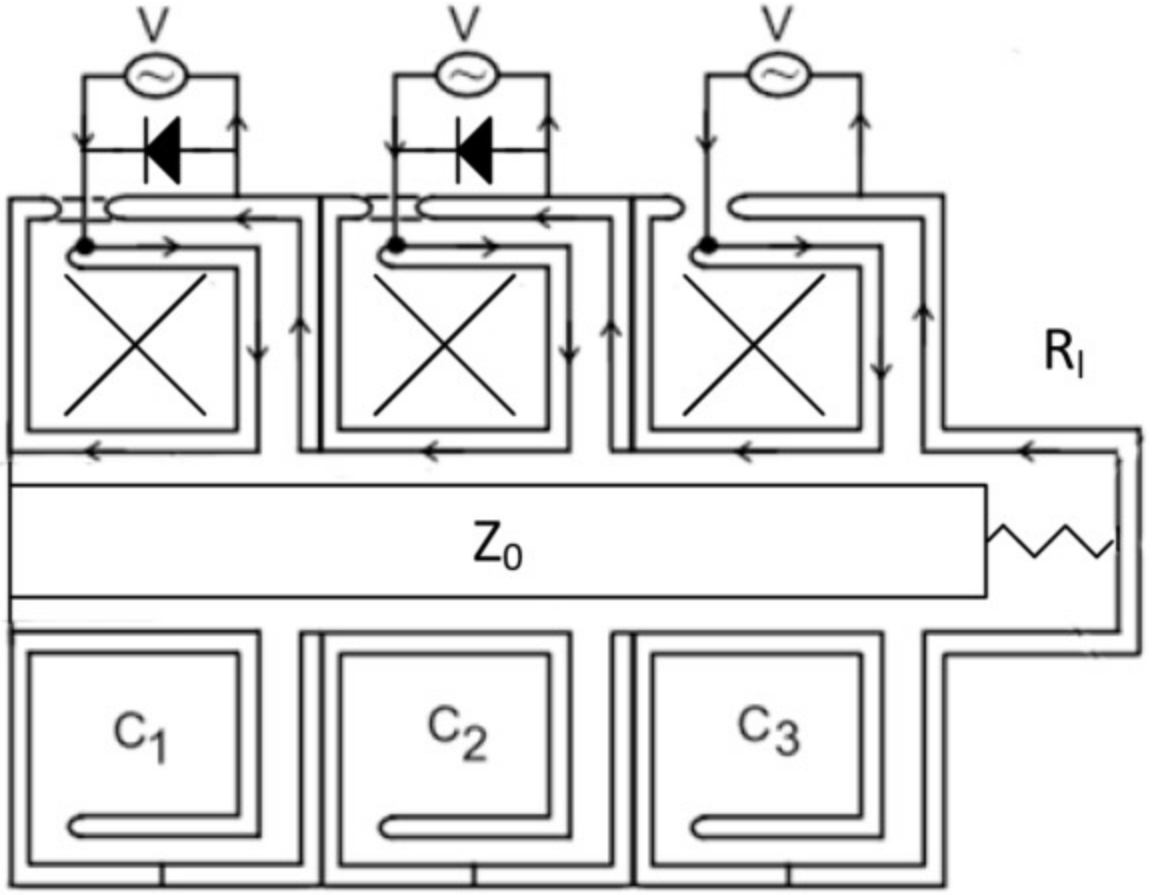


Other Commercial Suppliers

- Scandinova, Sweden
- Ampegon, Switzerland
- Jema, Spain
- Diversified Technologies, USA
- Others

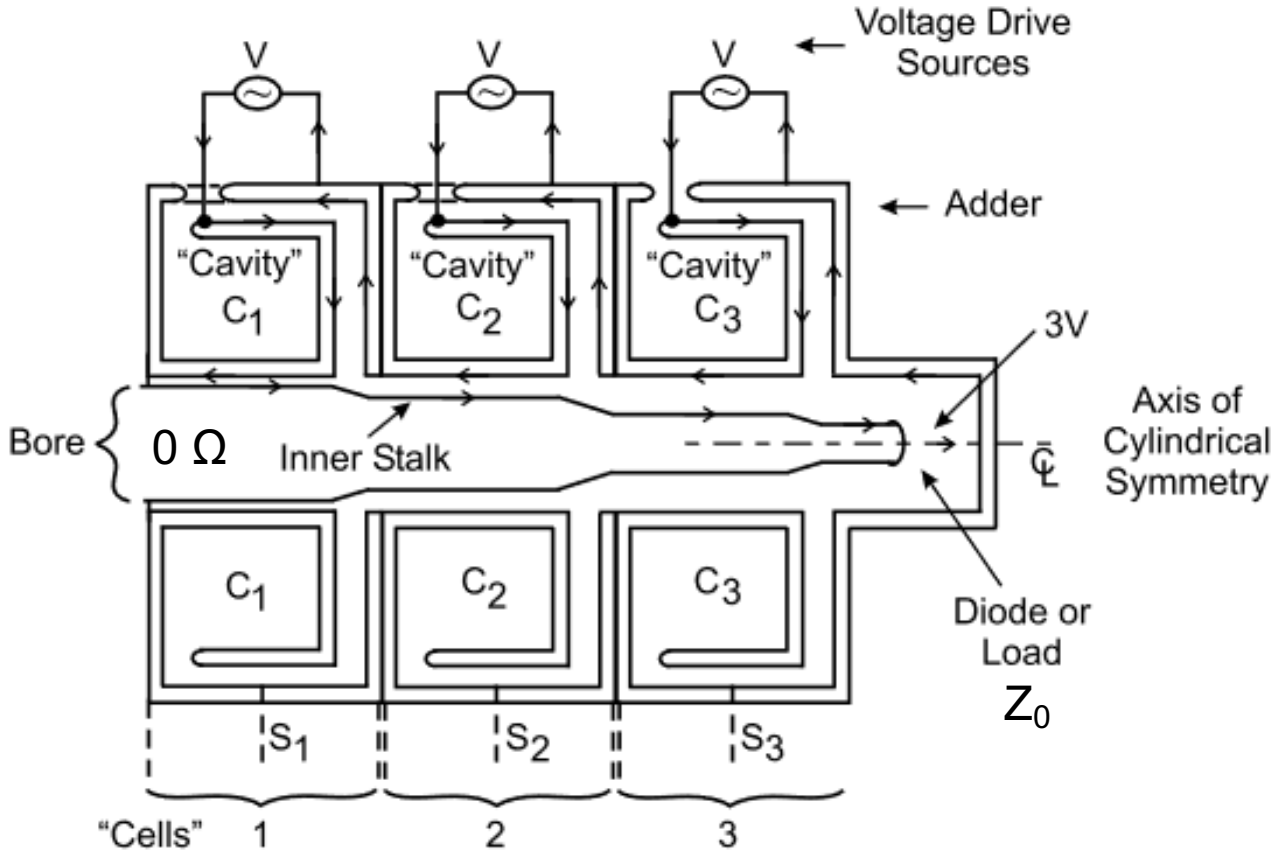
Reflections in the Structure

- Consider the structure shown, assuming $R_l=Z_0$ and only C_3 is driven. Diodes in C_1 and C_2 turn on, bypassing those cells and $V_o=V$.
- A wave propagates with an impedance of Z_0 /2 from C_3 to both the right and left, reflecting off a short on the left and R_l at the right.
- Wave continue to reflect, until damped by the load, effectively adding several propagation delays to the rise time.



Minimizing Reflections

- Tapering the adder secondary structure from Z_0 at the load end to 0 Ω at the shorted end will reduce the reflections and increase the rise time.
- Difficult to build tapers for bipolar adders.

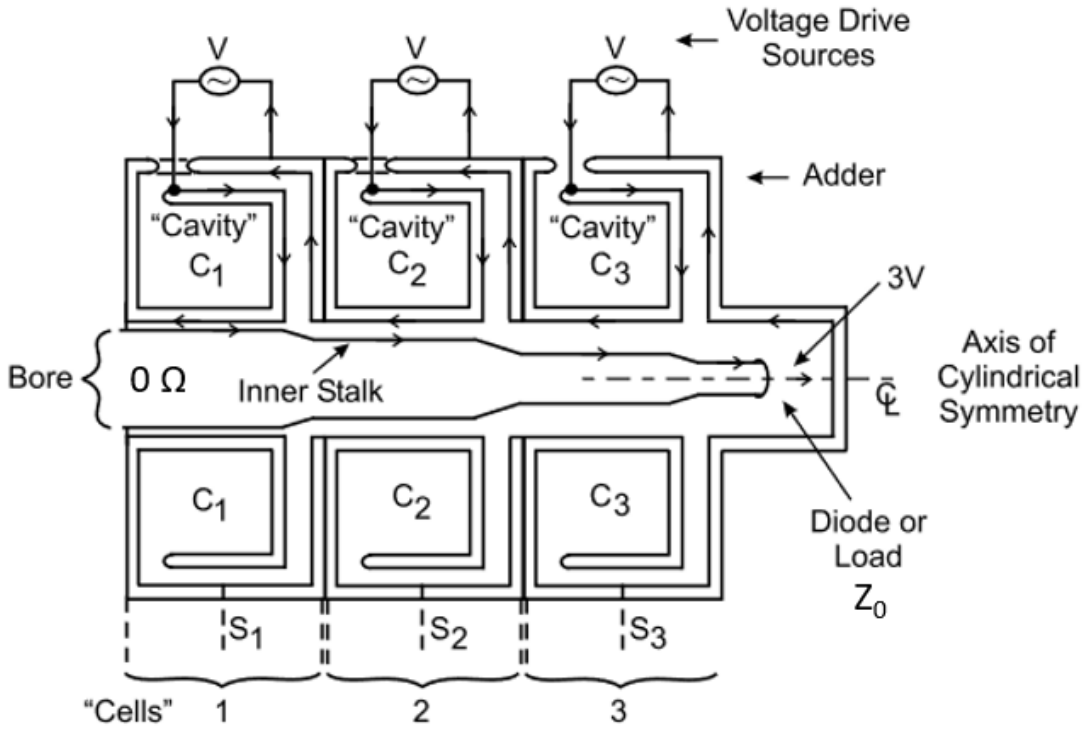


Delayed Triggering

- Delaying trigger of a cell to match the transmission to from the shorted end will minimize the rise time of the pulser.
- Trigger source for C1 first. At trigger C2.

$$t = \sqrt{L_p \frac{2\pi\varepsilon h}{ln\left(\frac{b}{a}\right)}}$$

- Trigger C3 delayed from C2 by the same amount.
- All wavefront arrive at the load at the same time.
- Only works for unipolar adder.



Design Example

- We have decided to use a solid state inductive adder to drive S-band klystrons with peak cathode voltages of 320 kV and peak current of 350 A. Pulses are 3 μs at 100 Hz with rise and fall times of less than 500 ns. Flat top requirement is ± 1% full scale.
- We need to:
  - Select which switches to use.
  - Determine how many cells are needed.
  - Select core material and design the cells for the adder.
  - Size and select the pulse capacitors.
- Is a step-up transformer needed? What should the turns ratio be?
- What rise time can you expect from the modulator?

Example: Switch Selection & Number of Cores

- Since peak and average power levels are fairly high, and the rise and fall times are moderate, a good choice for this design is to use IGBTs for switches.
- Would like to use highest power IGBTs available since that reduces the number of cells required. Could run into other constraints such as core size and cost.
- I chose Infineon FZ1200R45HL3_S7, 4.5 kV, 1200 A devices for this design to keep the number of cells and cores sizes moderate.
- For the 4.5 kV device I chose a maximum V_{CE} of 3200 V and a maximum I_E of 3200 A.

Example: Number of Adder Cells and Turns Ratio

- Adder output voltages and IGBT currents are shown below for various number of cells and secondary turns ratio.
- Voltage is calculated by VCE chosen times number of cells times turns ratio.
- IGBT current is calculated from the tube perveance at the calculated output voltage

Number of Cells	Vo with 5:1 Secondary	Vo with 6:1 Secondary	Vo with 7:1 Secondary	Vo with 8:1 Secondary	Ie with 5:1 Secondary	Ie with 6:1 Secondary	Ie with 7:1 Secondary	Ie with 8:1 Secondary
8	128000	153600	179200	204800	4.43E+02	6.98E+02	1.03E+03	1.43E+03
10	160000	192000	224000	256000	6.19E+02	9.76E+02	1.43E+03	2.00E+03
12	192000	230400	268800	307200	8.13E+02	1.28E+03	1.89E+03	2.63E+03
14	224000	268800	313600	**358400**	1.02E+03	1.62E+03	2.38E+03	**3.32E+03**
16	256000	307200	**358400**	409600	1.25E+03	1.98E+03	**2.90E+03**	4.05E+03
18	288000	**345600**	403200	460800	1.49E+03	**2.36E+03**	3.47E+03	4.84E+03
20	**320000**	384000	448000	512000	**1.75E+03**	2.76E+03	4.06E+03	5.67E+03

Chose 14 cell adder with 8:1 ratio.

Example: Core Selection & Size

- Core size is calculated from $Vs = N\Delta BA$, where V is the switch voltage, s is the pulse width, N is the number of primary turns, ΔB is the flux swing in the core and A is the cross sectional area of the core.
- Since the rise and fall times are relatively slow, I can use an iron based core material with thin laminations.
- For low core loss, I selected a tape wound Metglas 2605 SA1 material with a saturation flux of 1.56 T and assumed a stacking factor of 0.8. I assumed the core will be reset between pulses. For 1" ribbons I end up with a core cross section of 1" X 7.95".
- The magnetizing inductance contributes to droop and be calculated for a cell by $L_m = {}^{\mu A}/_{l_m}$ where μ is permeability of the core material A is the cross sectional area and l_m is the mean magnetic length.

Example: Capacitor Selection

- Neglecting the magnetizing inductance, we want less than 64 V (2 %) droop from the capacitor for 3200 A, 3 µs pulses, so the capacitor should be > 155 µF.
- We want capacitors with low ESR due to the peak currents which leads us to plastic film capacitors for such a large value. This is a good choice since they are stable and have low voltage coefficients.
- Available from a variety of manufacturers with a range of form factors.

Inductive Adder Example 2

Say we wanted to drive two klystrons with a single inductive adder:

Beam voltage, 420 kV

μ Perveance, 1.2 each

Pulse Width, 1.5 μs

PRF, 120 Hz

Using a two 6.5kV, 750 A switch per cell and an output transformer, how many cells should be used and what is the output transformer turns ratio?

Example 2

Switch selection – Infineon DD750S65K3, 6500 V, 750 A rated. Operate at 4000 V and 3000 A peak.

Equivalent perveance is 2.4 e^{-6} $A/V^{3/2}$ => Ilpeak=653 A. Maximum turn ratio of transformer is 6000 A/653 A=9. Therefore, the peak voltage from the adder is 47 kV.

For a 47 kV adder using switches operating at 4 kV, you need 12 cells.

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